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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,756	01/14/2004	Hajime Kimura	12732-0207001	1526

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
09/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/756,756	KIMURA ET AL.	
	Examiner	Art Unit	
	JEFF PIZIALI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,12,81 and 92-94* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,12,81 and 92-94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *21 July 2009* has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. *Claims 11, 12, 81, and 92-94* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Koyama et al (US 2001/0048408 A1)*** in view of ***Sundaresan (US 5,016,070 A)***.

Regarding claim 11, ***Koyama*** discloses a signal line driver circuit [*Fig. 1*] comprising:

a shift register [*Fig. 1; First - Third Shift Registers*];

a latch circuit [*Fig. 1; LAT Portion*], electrically connected to the shift register, comprising a plurality of pairs of current source circuits [*Fig. 5B*], wherein each of the plurality

of pairs of current source circuits includes a transistor having a gate, a source and a drain (*see Pages 5-6; Paragraphs 88-89*); and

a changing over circuit [*Fig. 1; 10a*] electrically connected to the plurality of pairs of current source circuits and a plurality of signal lines [*Fig. 1; S001 - S640*], wherein

each of the plurality of pairs of current source circuits is configured to control an output current value [*Fig. 5B; Output*] depending on a voltage between the gate and the source of the transistor of the pair of current source circuits that is generated by supplying a signal current [*Fig. 5B; Control Signals 1 & 2*] to the transistor while the gate and the drain of the transistor are electrically connected to each other (*see Pages 5-6; Paragraphs 88-89*),

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines, and

wherein the shift register is configured to output the set signal (*see Page 3; Paragraphs 50-53*).

Should it be shown that the ***Koyama*** reference teaches the instantly claimed "*latch circuit*" subject matter with insufficient specificity:

Sundaresan discloses a latch circuit [*Fig. 1; 10*], comprising a plurality of pairs of current source circuits [*Fig. 1; 12, 14, 16, 18, 48, 50*], wherein each of the plurality of pairs of current source circuits includes a transistor [*Fig. 1; 12, 14, 16, 18*] having a gate [*Fig. 1; 38, 40, 44, 46*], a source [*Fig. 1; 28, 30, 32, 34*] and a drain [*Fig. 1; 20, 22, 24, 26*]; wherein

each of the plurality of pairs of current source circuits is configured to control an output current value [*Fig. 1; via 42*] depending on a voltage between the gate and the source of the transistor of the pair of current source circuits that is generated by supplying a signal current [*Fig. 1; via 36*] to the transistor while the gate and the drain of the transistor are electrically connected [*Fig. 1; via 48, 50*] to each other (*see Column 2, Line 44 - Column 3, Line 42*).

Koyama and ***Sundaresan*** are analogous art, because they are from the shared inventive field of controlling SRAM latch circuitry.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Sundaresan's*** latch circuitry as ***Koyama's*** latch circuitry, because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predicable results to one of ordinary skill in the art at the time of the invention; and additionally

so as to make use of small SRAM cells that are unaffected by exposure to soft radiation.

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 11; furthermore, ***Koyama*** discloses a signal line driver circuit [*Fig. 6*] comprising:

a shift register [*Fig. 6; First - Third Shift Registers*]; a latch circuit [*Fig. 1; Latch Circuit Portion*], electrically connected to the shift register, comprising:

a plurality of pairs of current source circuits [*Fig. 5B*], wherein each of the plurality of pairs of current source circuits includes a transistor having a gate, a source and a drain (*see Pages 5-6; Paragraphs 88-89*);

a first switch (*see Fig. 5B*) provided between the shift register and each of the plurality of pairs of current source circuits (*see Pages 5-6; Paragraphs 88-89*); and

a second switch [*Fig. 6; 20*] (*see Page 6; Paragraphs 90-92*), and

a changing over circuit [*Fig. 6; 10c*] electrically connected between the plurality of pairs of current source circuits and a plurality of signal lines, wherein

each of the plurality of pairs of current source circuits is configured to control an output current value [*Fig. 5B; Output*] depending on a voltage between the gate and the source of the transistor of the pair of current source circuits that is generated by supplying a signal current [*Fig. 5B; Control Signals 1 & 2*] to the transistor while the gate and the drain of the transistor electrically are connected to each other (*see Pages 5-6; Paragraphs 88-89*),

wherein the changing over circuit is electrically connected [*e.g., Fig. 6: via Latch Circuit Portion, L001, BPC, PW-001, 20, DA-001, 10c*] to a particular pair of current source circuits through the second switch (*see Page 6; Paragraphs 92-93*),

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines,

wherein the shift register is configured to output the set signal, and

wherein the first and second switches are configured to be controlled by a latch pulse [*Fig. 1; LP*] (*see Page 3; Paragraphs 50-53*).

Regarding claim 81, this claim is rejected by the reasoning applied in rejecting claims 11 and 12; furthermore, ***Koyama*** discloses a signal line driver circuit [*Fig. 1*] comprising:

a plurality of current source circuits [*Fig. 5B*], wherein each of the plurality of current source circuits includes a transistor having a gate, a source and a drain (*see Pages 5-6; Paragraphs 88-89*),

wherein each of the plurality of current source circuits is configured to be supplied with a first current [*Fig. 5B; Input*] and to supply a second current [*Fig. 5B; Output*], and wherein a value of the second current depends on a voltage between the gate and the source of the transistor of the current source circuit that is generated by supplying the first current to the transistor while the gate and the drain are electrically connected to each other (*see Pages 5-6; Paragraphs 88-89*);

a plurality of signal lines [*Fig. 1; S001 - S640*]; and

a selector circuit [*Fig. 1; 10a*] electrically connected between the plurality of current source circuits and the plurality of signal lines, wherein the selector circuit is configured to select one of the plurality of signal lines to which the second current is supplied (*see Page 3; Paragraphs 50-53*).

Regarding claim 92, ***Sundaresan*** discloses a capacitor [*Fig. 1; 48, 50*] wherein one electrode of the capacitor is electrically connected to the source [*Fig. 1; 28, 32*] of the transistor [*Fig. 1; 12, 14*] and the other electrode of the capacitor [*Fig. 1; 48, 50*] is electrically connected

to the gate [*Fig. 1; 38, 44*] of the transistor [*Fig. 1; 12, 14*] (*see Column 2, Line 44 - Column 3, Line 42*).

Regarding claim 93, this claim is rejected by the reasoning applied in rejecting claim 92.

Regarding claim 94, this claim is rejected by the reasoning applied in rejecting claim 92.

Response to Arguments

8. Applicant's arguments filed *21 July 2009* have been fully considered but they are not persuasive.

Applicant's arguments with respect to *claims 11, 12, 81, and 92-94* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
24 September 2009